cant address bits for the trace memory corresponding to successive cycles of operation.

5. An apparatus according to claim 1, wherein said memory retrieval means comprises an address setting switch, an address comparator having inputs connected to the address setting switch and the address command bus, a latch register responsive to the address comparator and connected to the data bus for receiving the retrieved data and transitional record, and a D/A converter connected to the latch output for generating an analog signal to operate the record generating means.

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